Hard Switching Losses Calculations

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This document intends to provide an easy implementation for switching loss calculations for hard-switching converters. These formulas are well-known in the industry, but particular care has been taken to provide the best implementation considering the data normally provided in power semiconductors datasheets. The formulas used are generic and can be applied to eMode Gan FETs as well as Si MOSFETs. We only cover the losses linked to the transition events, since conduction losses are quite easy to calculate.

The use of these formulas is intended to help design engineers in the component selection process and to compare different devices in application conditions. This is why we limit the calculations to use data available commonly in Si MOSFETs and GaN FETs datasheets.

This simplified approach is not suitable in most cases for an accurate prediction of system efficiency. More accurate mixed mode simulations (Spice, Thermal Finite Element Analysis, etc..), and eventually the real world, should be used for that purpose.

1.0 Assumptions

With the goal of calculating losses for a general half-bridge configuration shown in Figure 1, we break down the process in 4 steps.

Firstly, overlap losses, where current and voltage are present simultaneously, can be calculated from the simplified transition events shown in Figure 2 and Figure 3.

Second, output capacitance losses are considered: the charging and discharging of this capacitor generates losses in the resistance of the current path.

Third, reverse recovery losses are calculated in case when MOSFETs are used (GaN FETs do not have these losses), including the resistive losses associated with these currents.

Lastly, gate drive losses are considered, even if most of them are dissipated externally to the switch in the gate drive circuit.

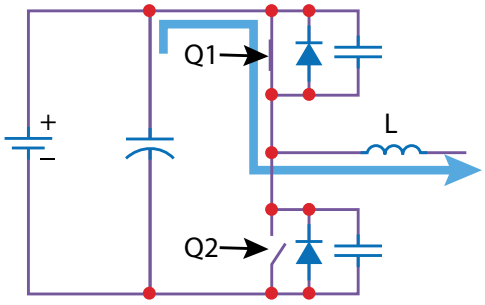

Figure 1 - Hard switched half bridge

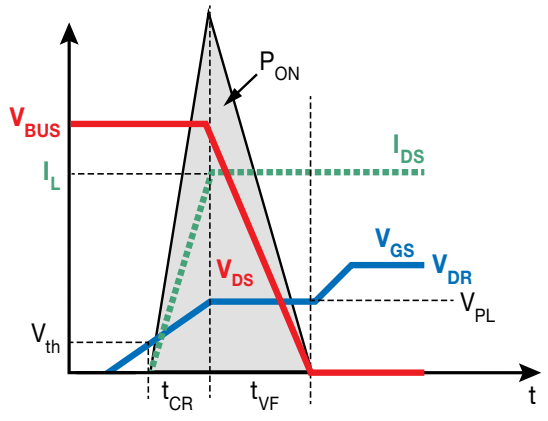

Figure 2 - Turn on simplified waveform

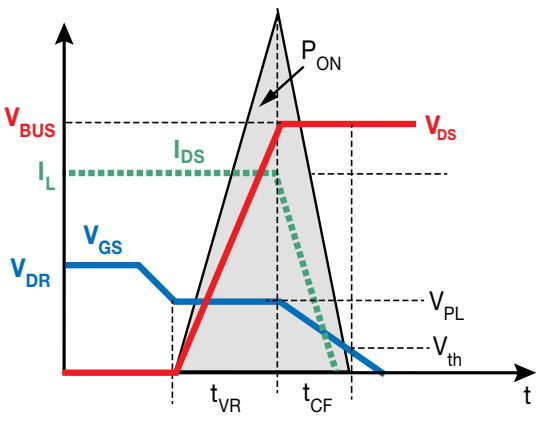

Figure 3 - Turn off simplified waveform

The gate charge nomenclature shown in Figure 4 is utilized.

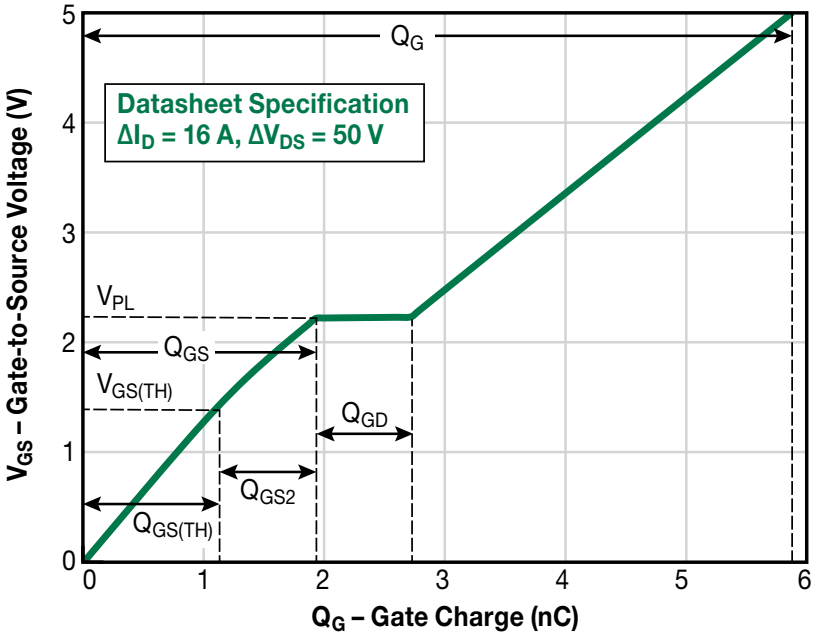

Figure 4 - Gate charge nomenclature

2.0 Overlap Losses

In the circuit analyzed (Figure 1), overlap losses take in place in switch Q1. Switch Q2 does not have overlap losses.

2.1 Turn on Losses

From Figure 2, these losses can be easily calculated based on the transition times.

$$E_{ol,ON,Q1}(V,I,Tj) = \frac{1}{2} \cdot V_{bus} \cdot I_L \cdot \left(t_{cr,ON} + t_{vf,ON}\right) \quad \text{Eq. 1}$$

2.1.1 Current Rise Times

The current rise time can be calculated based on the gate drive current $I_{GC,on}$ and the gate charge Q_{GS2} needed to bring the gate voltage from the threshold voltage to the Miller Plateau (see Figure 4), to be calculated in the specific turn on conditions:

$$t_{cr,ON} = \frac{Q_{GS2}(I,T_J)}{I_{GC,cr,ON}(I,T_J)} \quad \text{Eq. 2}$$

The gate charge calculation start with the $Q_{GS2,ds}$ in the datasheet conditions:

$$Q_{GS2,ds} = Q_{GS,ds} - Q_{GS,th,ds} \quad \text{Eq. 3}$$

Where $Q_{GS,ds}$ and $Q_{GS,th,ds}$ are either given in the datasheet tables or can be calculated from the gate charge curve in the figures section. These are given at a specific current $I_{D,specQg}$, and at 25°C.

The Q_{GS2} (I,T_J) in the specific operating conditions can be linearly scaled from the value in the original conditions with the following formula since both V_{th} $(T_J)$and V_{pl} $(I,T_J)$are changing:

$$Q_{GS2}(I,T_J) = Q_{GS2,ds} \cdot \frac{V_{pl}(I,T_J) - V_{th}(T_J)}{V_{pl}(I_{D,specQg}, 25°C) - V_{th}(25°C)} \quad \text{Eq. 4}$$

V_{th} (T_J) can be calculated from the V_{th}(T_J) curve like the one in Figure 5. While the Miller plateau V_{pl} (I,T_J) can be calculated by interpolating the transfer curves like the ones in Figure 6.

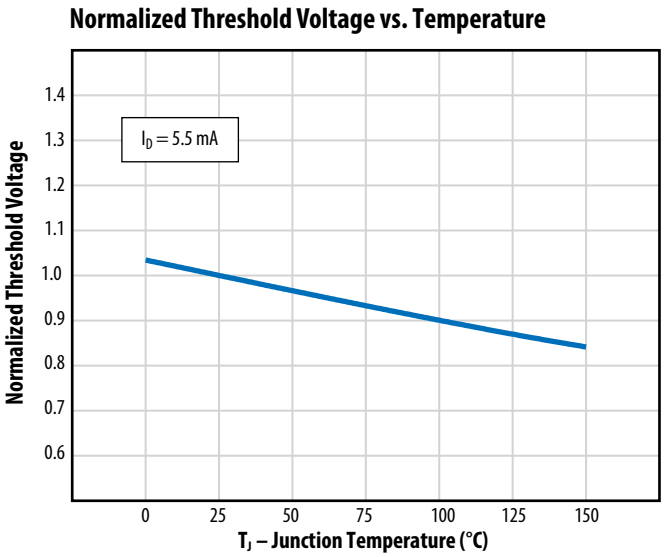

Figure 5 - V_{th} vs. T_J for EPC2619

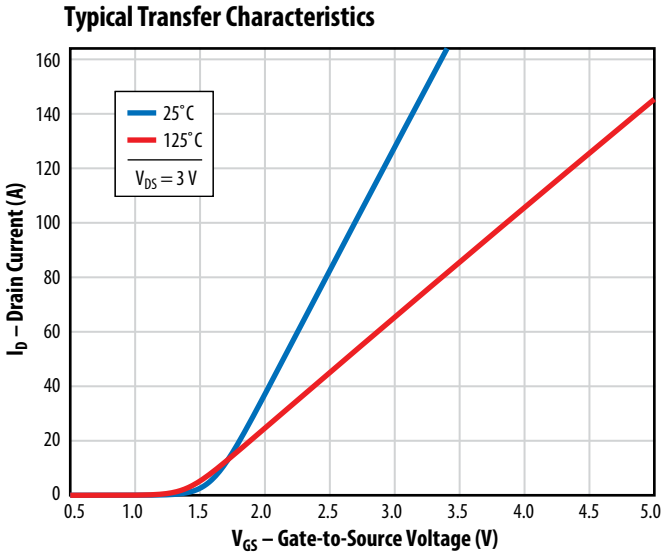

Figure 6 - Transfer curves for EPC2619

The gate drive current can be calculated by using the average voltage on the gate during this transition as such:

$$I_{GC,cr,ON}(I,T_J) = \frac{V_{DR} - \left(\frac{V_{Pl}(I,T_J) + V_{th}(T_J)}{2}\right)}{R_{Gon}} \quad \text{Eq. 5}$$

Where V_{DR} is the turn on gate drive voltage and R_{Gon} is the total gate resistance in the turn on gate drive loop, typically the sum of the gate driver pull-up resistance, the external turn on gate resistor and the internal device gate resistance.

2.1.2 Voltage Fall Time

The voltage fall time can be calculated with the assumption that the gate voltage stays fixed at $V_{Pl,Q1}$ (I,T_J). Then the gate drive current needs to charge the gate to drain capacitance:

$$t_{vf,ON} = \frac{Q_{GD}(V)}{I_{GC,vf,ON}(I,T_J)} \quad \text{Eq. 6}$$

It is important to use the charge here as the capacitances of power devices are very non-linear. The charge can be calculated by integrating the capacitance curve C_{RSS}(v) like the ones in Figure 7:

$$Q_{GD}(V_{bus}) = \int_0^{V_{bus}} C_{RSS}(v) \cdot dv = \sum_{k=1}^{k(V_{bus})} \frac{C_{RSS}(k) + C_{RSS}(k-1)}{2} \cdot \left(V_{DS}(k) - V_{DS}(k-1)\right) \quad \text{Eq. 7}$$

Where the curve in Figure 7 has been digitized in k points.

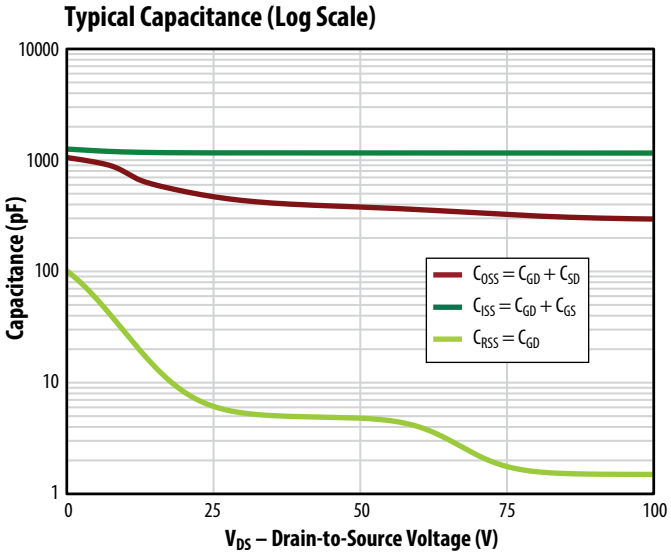

Figure 7 - Capacitance curves from EPC2619

The gate drive current $I_{GC,vf,ON}$ (I,T_J) can be calculated by using the simple equation:

$$I_{GC,vf,ON}(I,T_J) = \frac{V_{DR} - V_{Pl,Q1}(I,T_J)}{R_{Gon}} \quad \text{Eq. 8}$$

Where $V_{Pl,Q1}$ (I,T_J) and R_{Gon} are the ones from the previous current rise time calculations in 2.1.1.

Where V_{DR} is the turn on gate drive voltage and R_{Gon} is the total gate resistance in the turn on gate drive loop, typically the sum of the gate driver pull-up resistance, the external turn on gate resistor and the internal device gate resistance.

2.2 Turn Off Losses

From Figure 3, these losses can be also calculated based on the transition times via the equation:

$$E_{ol,OFF,Q1}(V,I,Tj)\& = \frac{1}{2} \cdot V \cdot I \cdot \left(t_{cf,OFF} + t_{vr,OFF}\right) \quad \text{Eq. 9}$$

2.2.1 Current Fall Time

The current fall time can be calculated similarly to the current rise time in section 2.1.1, but in the turn off conditions (mainly turn off current).

$$t_{cf,OFF} = \frac{Q_{GS2}(I,T_J)}{I_{GC,cf,OFF}(I,T_J)} \quad \text{Eq. 10}$$

The calculation of Q_{GS2} (I,T_J) follows the same procedure as outline in section 2.1.1., but in the new turn off conditions.

Then the gate drive current $I_{GV,cf,Off}$ (I,T_J) can be calculated by using the average voltage on the gate during this transition as such:

$$I_{GC,cf,OFF}(I,T_J) = \frac{\left(V_{Pl,Q1}(I,T_J) + V_{th}(T_J)\right)/2}{R_{Goff}} \quad \text{Eq. 11}$$

Assuming 0 V turn off, which is recommended for GaN FETs. $V_{Pl,Q1}$ (I,T_J) is the same one found during the Q_{GS2} (I,T_J) calculation, and R_{Goff} is the total gate resistance in the gate drive loop during turn off, typically the sum of the gate driver pull-down resistance, the external turn off gate resistor (which can be different than the turn on one), and the internal device gate resistance.

2.2.2 Voltage rise time

The voltage rise time can be calculated is a similar way to the voltage fall time in 2.1.2, with the assumption that the gate voltage stays fixed at $V_{Pl,Q1}(I,T_J)$. Then the gate drive current needs to charge the gate to drain capacitance:

$$t_{vr,OFF} = \frac{Q_{GD}(V)}{I_{GC,vr,OFF}(I,T_J)} \quad \text{Eq. 12}$$

The Q_{GD} (V) calculation is the same as in section 1, while the gate drive current $I_{GC,vr,OFF}(I,T_J)$ can be calculated by using the simple equation:

$$I_{GC,vr,OFF}(I,T_J) = \frac{V_{Pl,Q1}(I,T_J)}{R_{Goff}} \quad \text{Eq. 13}$$

Assuming 0 V turn off, which is recommended for GaN FETs. $V_{Pl,Q1}(I,T_J)$ is the same one found during the $Q_{GS2}(I,T_J)$ calculation in section 2.2.1, and R_{Goff} is the total gate resistance in the gate drive loop during turn off, typically the sum of the gate driver pull-down resistance, the external turn off gate resistor (which can be different than the turn on one), and the internal device gate resistance.

2.3 Summary of Overlap Losses Formulas

$$\begin{aligned} E_{ol,ON,Q1}(V,I,Tj) &= \frac{1}{2}\cdot V\cdot I\cdot\left(t_{cr,ON}+t_{vf,ON}\right)\\ &= \frac{1}{2}\cdot V\cdot I\cdot\left(\frac{Q_{GS2}(I,T_J)}{I_{GC,ON}(I,T_J)}+\frac{Q_{GD}(V)}{I_{GC,ON}(I,T_J)}\right)\\ &= \frac{1}{2}\cdot V\cdot I\cdot\left(\frac{Q_{GS2}(I,T_J)}{\frac{V_{DR}-\left(\frac{V_{Pl}(I,T_J)+V_{th}(T_J)}{2}\right)}{R_{Gon}}}+\frac{Q_{GD}(V)}{\frac{V_{DR}-V_{Pl,Q1}(I,T_J)}{R_{Gon}}}\right) \end{aligned}$$

$$\begin{aligned} E_{ol,OFF,Q1}(V,I,Tj) &= \frac{1}{2}\cdot V\cdot I\cdot\left(t_{cf,OFF}+t_{vr,OFF}\right)\\ &= \frac{1}{2}\cdot V\cdot I\cdot\left(\frac{Q_{GS2}(I,T_J)}{I_{GC,OFF}(I,T_J)}+\frac{Q_{GD}(V)}{I_{GC,OFF}(I,T_J)}\right)\\ &= \frac{1}{2}\cdot V\cdot I\cdot\left(Q_{GS2}(I,T_J)\Big/\frac{\left(\frac{V_{Pl,Q1}(I,T_J)+V_{th}(T_J)}{2}\right)}{R_{Goff}}+Q_{GD}(V)\Big/\frac{V_{Pl,Q1}(I,T_J)}{R_{Goff}}\right) \end{aligned} \quad \text{Eq. 14}$$

3.0 Output capacitance losses

The first issue to address is the non-linearity of the output capacitances of both Si MOSFETs and GaN FETs, which means the simple formula $E = {}^1/_2 \cdot C \cdot V^2$) for a fixed capacitance cannot be used. The best approach for loss calculation is to integrate the capacitance curves from Figure 7:

$$E_{OSS}(V) = \int_0^{V_{bus}} C_{OSS}(v)\cdot v.dv = \sum_{k=1}^{k(V_{bus})} \frac{C_{OSS}(k)+C_{OSS}(k-1)}{2}\cdot\left(V_{DS}(k)-V_{DS}(k-1)\right)\cdot V_{DS}(k) \quad \text{Eq. 15}$$

Since capacitances can store energy, a detailed analysis is needed to distinguish between energy storage and energy dissipation. The following analysis is for the half-bridge converter from Figure 1.

First during the switch node falling transition (high side turn off), $C_{OSS,Q1}$ is charged by the inductor current ($E_{OSS,Q1}$), while $C_{OSS,Q2}$ energy ($E_{OSS,Q2}$) is discharged and recovered to the load.

Second, in the switch note rising transition (high side turn on), the energy stored in $C_{OSS,Q1}$ ($E_{OSS,Q1}$) is dissipated in the channel of Q1. Moreover $C_{OSS,Q2}$ is charged from the V_{bus} (energy that will be later recovered). In this situation the bus will provide the total energy $V_{bus} \cdot Q_{OSS,Q2}$ (which includes the energy stored in Q2, as well as the energy dissipated in the resistance of the charging path).

$$E_{bus} = \int_0^{V_{bus}} i(t) \cdot dt = \int_0^{V_{bus}} \frac{dq_{Q2}(t)}{dt} \cdot dt = V_{bus} \cdot Q_{OSS,Q2} \quad \text{Eq. 16}$$

Overall:

$$E_{OSS} = V_{bus} \cdot Q_{OSS,Q2} + \mathrm{E_{OSS,Q1}} - \mathrm{E_{OSS,Q2}} \quad \text{Eq. 17}$$

In case of a symmetrical half-bridge, this can be simplified to

$$E_{OSS} = V_{bus} \cdot Q_{OSS,Q2} \quad \text{Eq. 18}$$

Which are added to the high side Q1 overlap losses.

4.0 Reverse Recovery Losses

Reverse recovery losses are difficult to model and calculate, although they can be a significant contributor to losses for Si MOSFETs, while they do not happen for GaN FETs.

For Si MOSFETs we need to rely on the datasheet parameters which often specify Q_{RR} in a single condition, not always relevant to the actual application conditions.

Reverse recovery happens during the switch node positive voltage transition, where Q_{RR} is provided to Q2 from V_{bus}.

The overall losses can be calculated as:

$$E_{RR,total} = V_{bus} \cdot Q_{RR} \quad \text{Eq. 19}$$

5.0 Gate Drive Losses

The power losses associated with the gate charge can be calculated as:

$$E_G = Q_G \cdot V_{DR} \quad \text{Eq. 20}$$

Where Q_G is given in the datasheet as defined in Figure 4. These losses are dissipated in the 3 resistors of the gate loop which are the pull-up/down resistance of the gate driver, the turn on/off gate resistors and the device internal resistor. Therefore, in most cases these losses happen outside the device.